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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,990	03/24/2004	Samson Huang	42P15059D	6775

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EXAMINER	
XIAO, KE	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,990	HUANG ET AL.	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15,17 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15,17 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama (US 7,088,322) in view of Yamazaki (US 7,053,973).

Regarding **Claim 15**, Koyama teaches a liquid crystal on silicon imaging device (Koyama, Fig. 20), comprising:

a cover glass (Koyama, Fig. 10B element 1009);

a silicon backplane physically connected to the cover glass in a connection area, the connection area defined by a generally rectangular adhesive strip (Koyama, Fig. 10B Col. 5 lines 20-35); and

a liquid crystal sealed between the cover glass and the silicon backplane by the adhesive strip (Koyama, Fig. 10B element 1010 and 1008);

wherein the silicon backplane comprises:

a frame buffer configured to store pixel data (Koyama, Fig. 20 element 2009);

a pixel array located completely within the connection area (Koyama, Figs. 10 and 20 elements 1002 and 2007);

an interface control block connected between the frame buffer and the pixel array, the interface control block being adapted to determined pulse amplitude modulation waveforms for the pixel array in accordance with the pixel data stored in the frame buffer (Koyama, Fig. 20 element 2005 and 2006);

an external interface block data, configured to provide external interface to the device, including receiving pixel data and transferring the received pixel data into the frame buffer (Koyama, Fig. 20 element 2008); and

a control block data, connected to the external interface block, the frame buffer, and the interface control block, the control circuit being adapted to provide control signals to operate the device (Koyama, Fig, 20 element 2002);

wherein at least a portion of the frame buffer block includes memory cells within the same connection area as pixel elements of the pixel array (Koyama, Figs. 10a and 20 memory portions, clearly the memory portions are *within* the sealing area as shown in Fig. 10a which as per the applicant's arguments satisfies the limitations of "co-located" as well as "within the same connection area" as claimed).

Koyama fails to teach that the frame buffer, external interface block, and control block are all located at least partially under the adhesive strip. Yamazaki teaches that use of the sealing agent over the *entire area* of the display device *except* the pixel portion (Yamazaki, Fig. 1 element 105).

It would have been obvious to use the sealing method of Yamazaki in the device of Koyama in order to provide extra protection to the circuits located integral to the semiconductor display device.

Koyama in view of Yamazaki also fails to teach determining pulse width modulation waveforms but instead teaches pulse amplitude modulation using varied voltages. The examiner takes official notice that pulse width modulation is a well known method of driving a liquid crystal display as opposed to or even in combination with pulse amplitude modulation. It would have been obvious to one of ordinary skill in the art at the time of the invention to add pulse width modulation to the display device of Koyama in view of Yamazaki in order to provide a wider range of gray scale driving.

Regarding **Claim 17**, Koyama further teaches that the frame buffer includes a front buffer and a back buffer (Koyama, Fig. 20 elements 2003 and 2004).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama (US 7,088,322) in view of Yamazaki (US 7,053,973) as applied to Claims 15-17 above, and further in view of Negishi (US 5,907,314).

Regarding **Claim 19**, Koyama in view of Yamazaki fails to teach dividing up the display components as claimed. Negishi teaches two independent display systems can be put on a single substrate (Negishi, Figs. 10 and 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to duplicated the display system of Koyama in view of Yamazaki as taught by Negishi in order to provide independent control to a top half and a bottom half of the display.

Response to Arguments

Applicant's arguments filed November 9th, 2009 have been fully considered but they are not persuasive.

Regarding independent Claim 15, the applicant argues that prior art fails to teach "wherein at least a portion of the frame buffer block includes memory cells within the same connection area as pixel elements of the pixel array". Specifically the applicant cites the instant application "some embodiments of the invention include portions of the first and second frame buffers FBB1 45 and FBB2 49), the associated first and second interface blocks (ICB1 46 and ICB2 48) and the control block (CB 43) located on the periphery of the die 40 and at least partially located within the area under an adhesive strip 41 that attaches the cover glass to the die 40 thus saving valuable die size. If the size and complexity of the device permits, it is preferable that the frame buffers are located completely within the area under the adhesive strip 41, thus providing increased functionality with no increase in die size" and Fig. 4 FBB1 and FBB2 stating that the memory portions of Koyama are located adjacent to the pixel region and not "within the same connection area" as claimed. The examiner respectfully disagrees; the term "within the same connection area" is not specifically defined in the specification. The examiner is therefore, able to reasonably interpret "within the same connection area" to be on the same substrate. If the connection area is considered the entire substrate then both the memory portion as well as the pixel portion are both within the same connection area.

However for the sake of argument even if the interpretation was based on the narrow description of the specification as pointed out by the applicant the rejection would still be proper. The examiner notes that Fig. 4 as well as the accompanying description of the instant application when taken together to define "within the same connection area" only call for the memory portions to be within a sealing region of the display substrate along w/ the pixel portion, this is clearly shown in Fig. 4 where the sealing region surrounds the portion which is "within the same connection area" including the memory portion as well as the pixel portion which are *adjacent* to one another. Thus the current rejection as further explained by the examiner with the inclusion of Fig. 10a along with Fig. 20 satisfies the definition given by the applicant.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571)272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Ke Xiao/
Examiner, Art Unit 2629